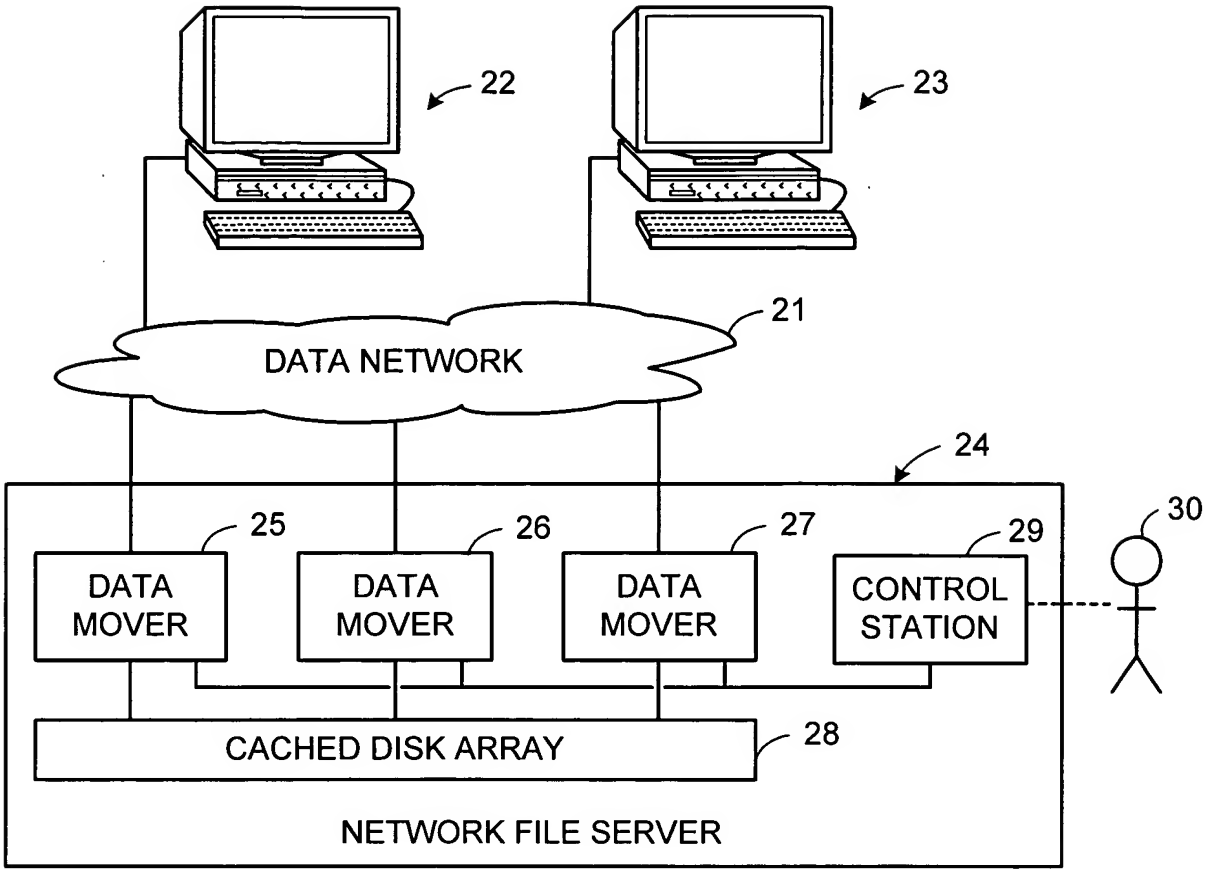

FIG. 1

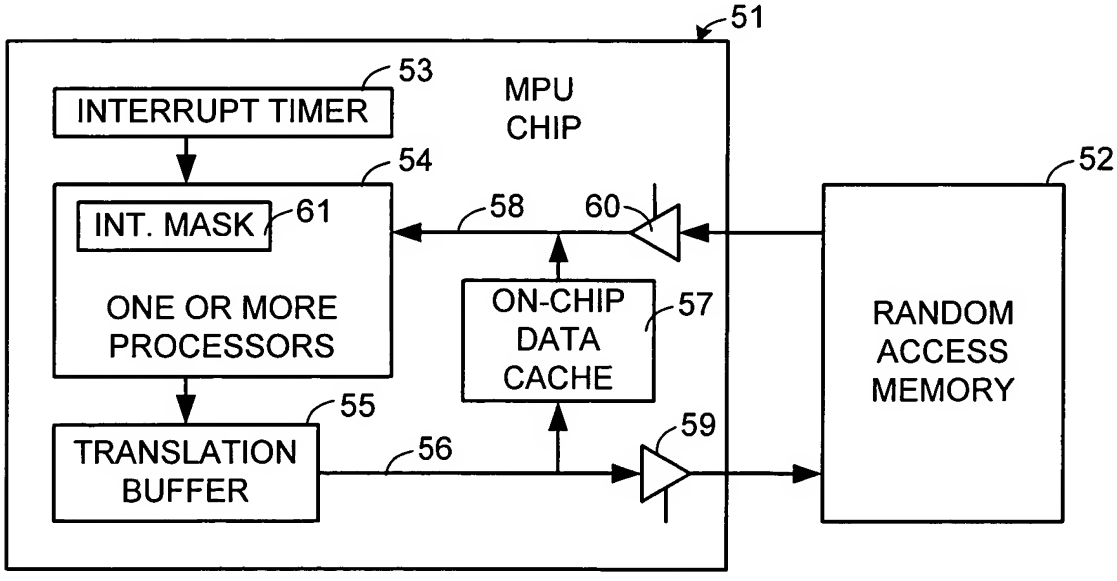

FIG. 3 (PRIOR ART)

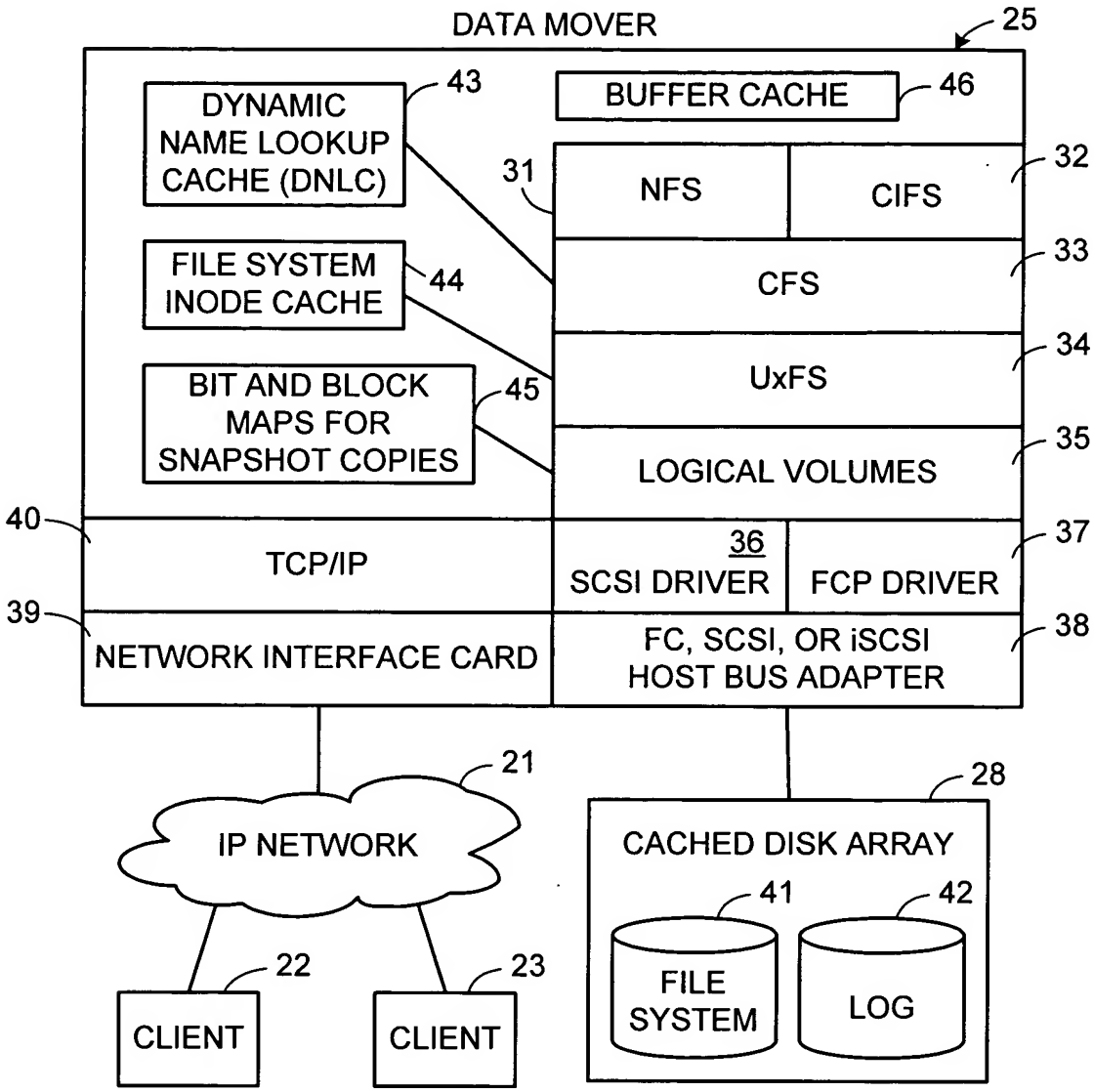

FIG. 2

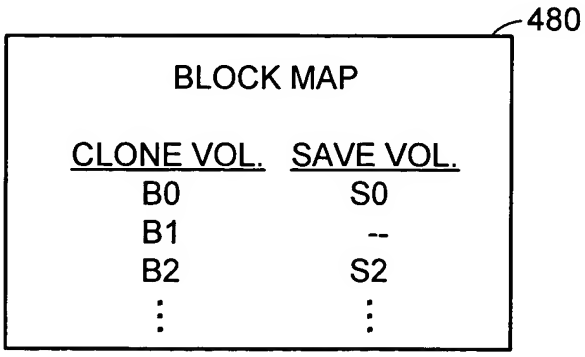

FIG. 8
(PRIOR ART)

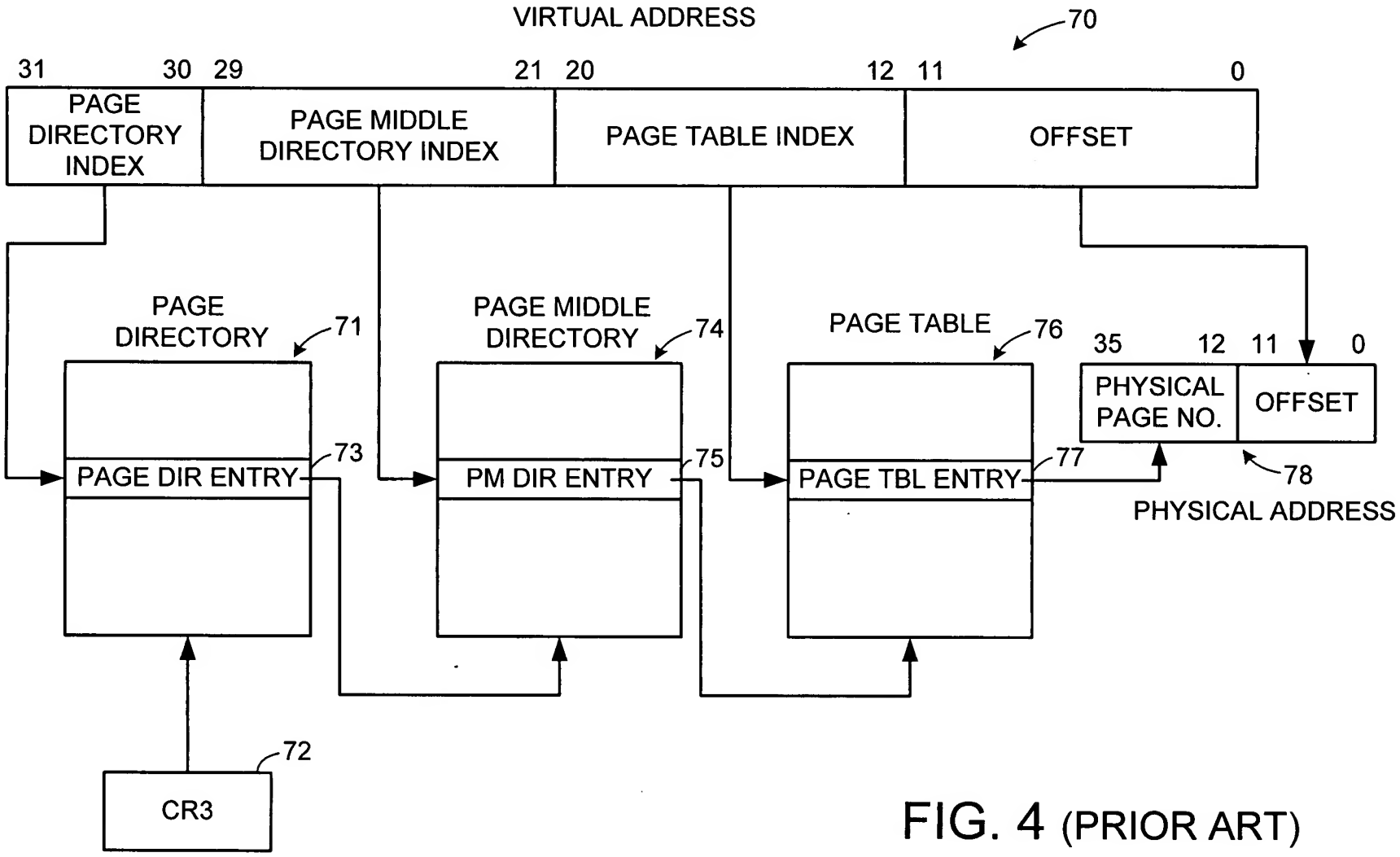

FIG. 4 (PRIOR ART)

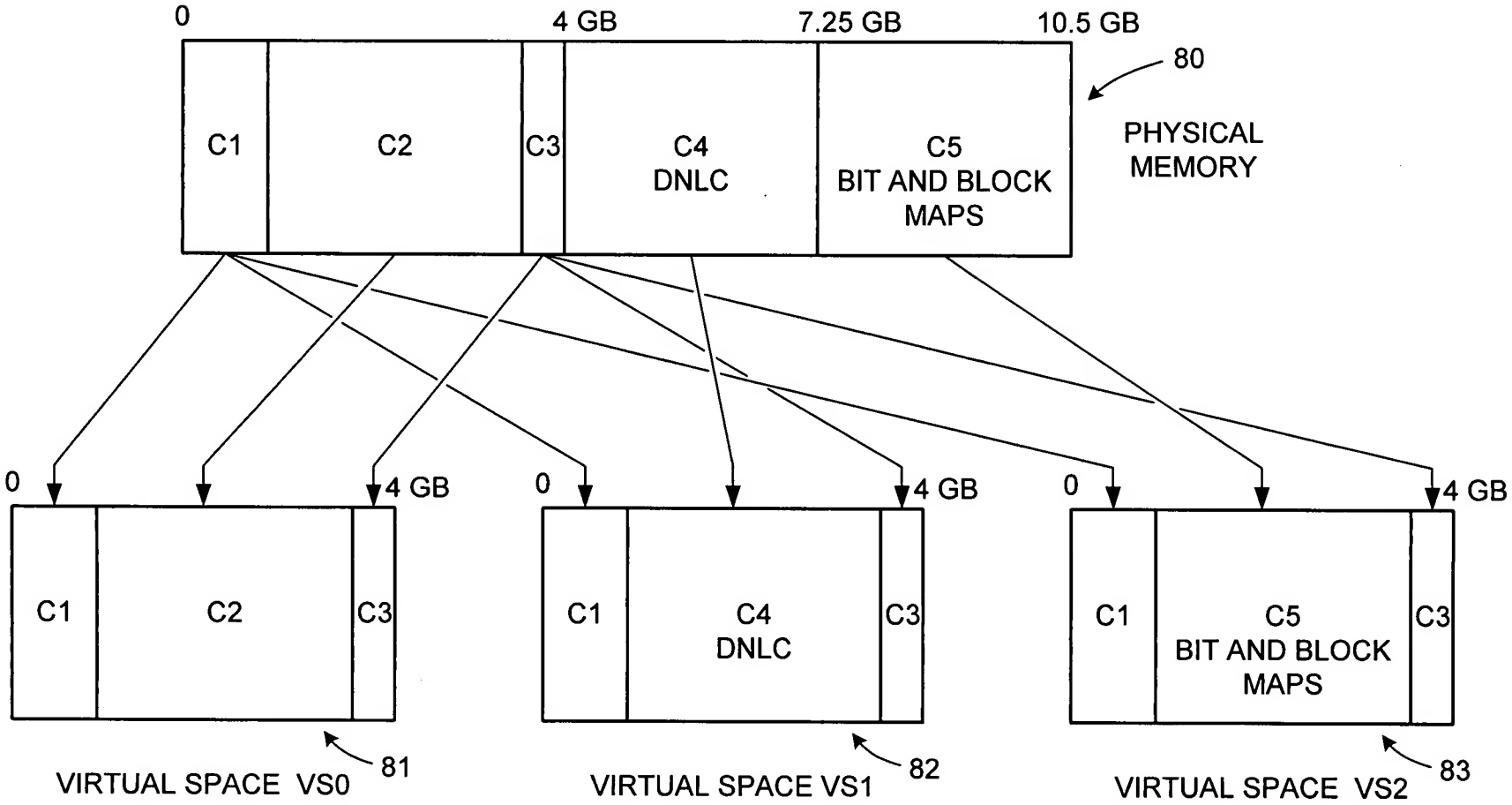
0
4 GB
7.25 GB
10.5 GB
80
C1
C2
C3
C4
DNLC
C5
BIT AND BLOCK
MAPS
PHYSICAL
MEMORY
0
4 GB
C1
C2
C3
VIRTUAL SPACE VS0
81
0
4 GB
C1
C4
DNLC
C3
VIRTUAL SPACE VS1
82
0
4 GB
C1
C5
BIT AND BLOCK
MAPS
C3
VIRTUAL SPACE VS2
83

FIG. 5

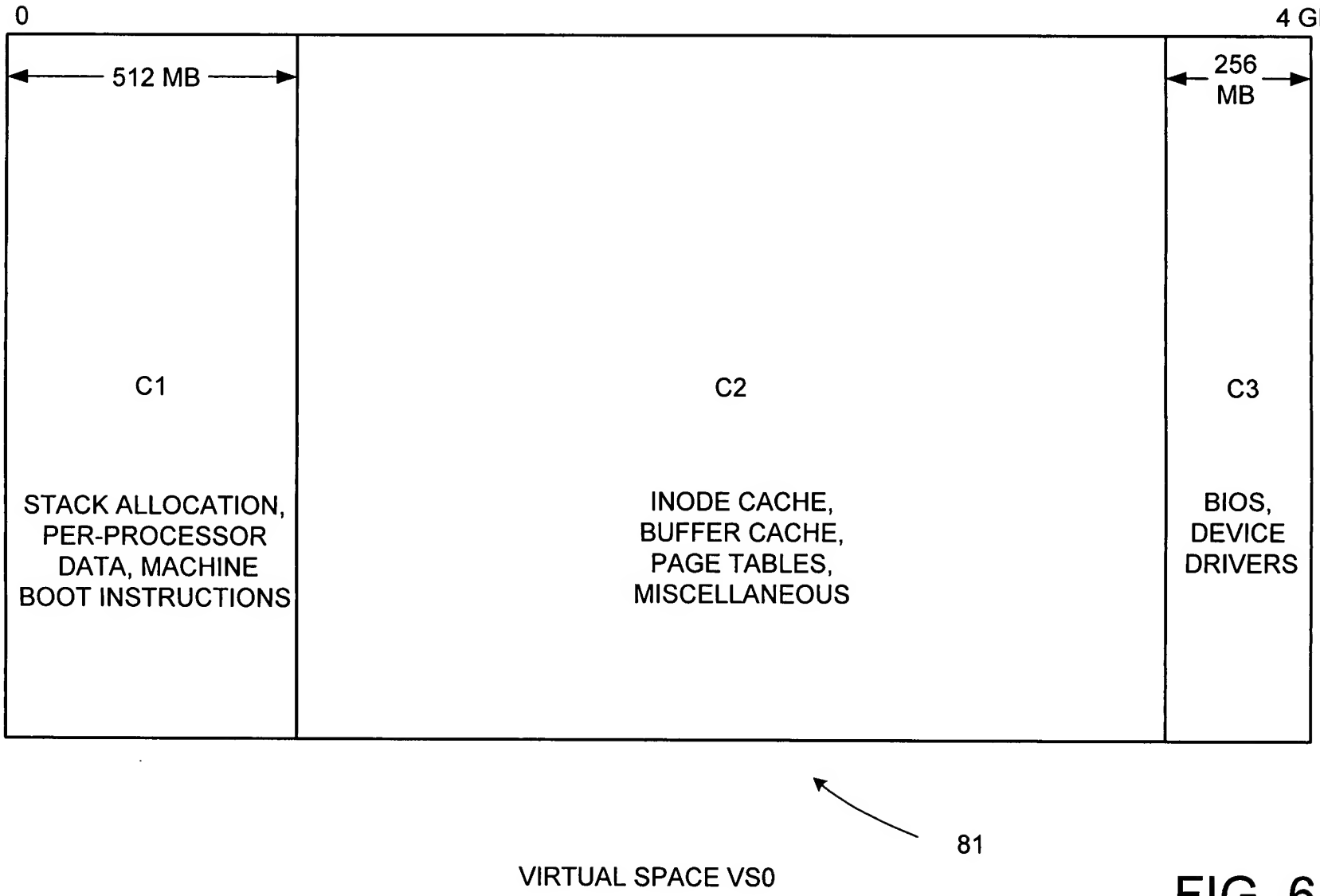
0
4 GB
512 MB
256 MB
C1
C2
C3
STACK ALLOCATION, PER-PROCESSOR DATA, MACHINE BOOT INSTRUCTIONS
INODE CACHE, BUFFER CACHE, PAGE TABLES, MISCELLANEOUS
BIOS, DEVICE DRIVERS
81
VIRTUAL SPACE VS0

FIG. 6

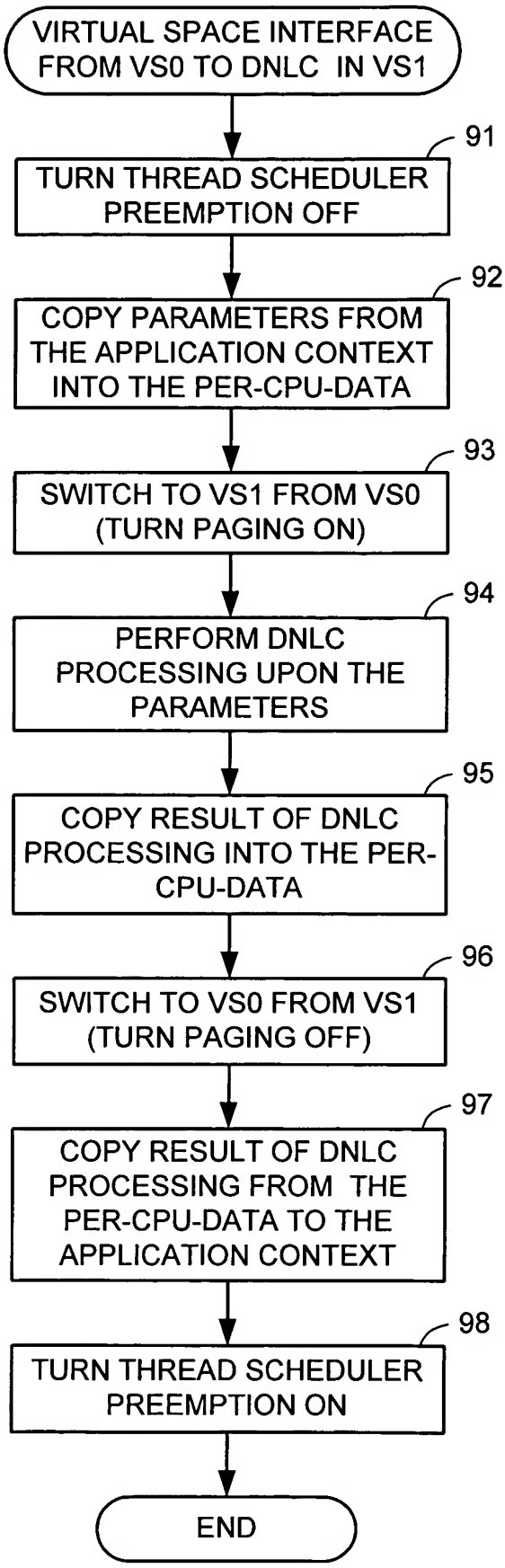
VIRTUAL SPACE INTERFACE FROM VS0 TO DNLC IN VS1
91
TURN THREAD SCHEDULER PREEMPTION OFF
92
COPY PARAMETERS FROM THE APPLICATION CONTEXT INTO THE PER-CPU-DATA
93
SWITCH TO VS1 FROM VS0 (TURN PAGING ON)
94
PERFORM DNLC PROCESSING UPON THE PARAMETERS
95
COPY RESULT OF DNLC PROCESSING INTO THE PER-CPU-DATA
96
SWITCH TO VS0 FROM VS1 (TURN PAGING OFF)
97
COPY RESULT OF DNLC PROCESSING FROM THE PER-CPU-DATA TO THE APPLICATION CONTEXT
98
TURN THREAD SCHEDULER PREEMPTION ON
END

FIG. 7

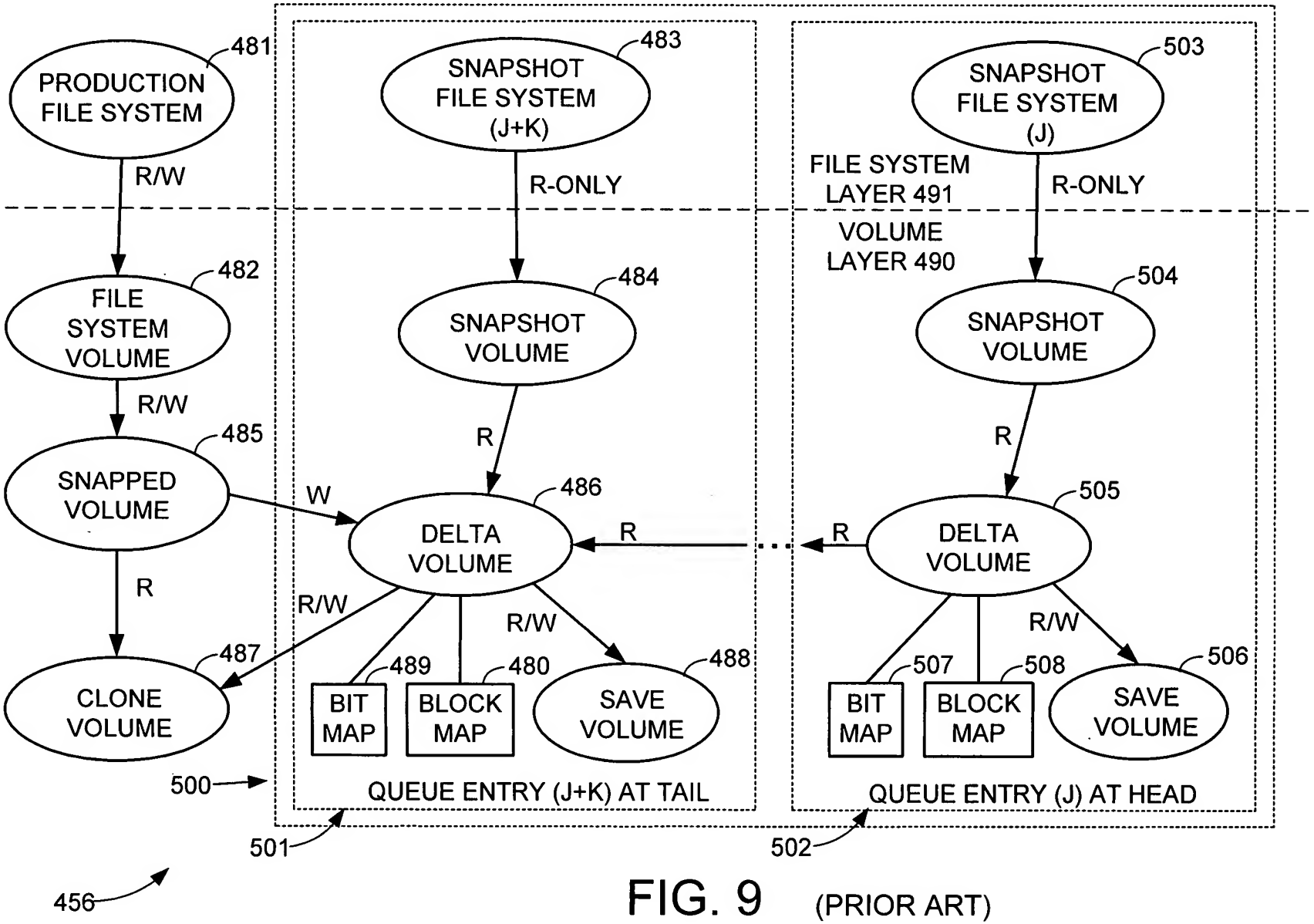

FIG. 9 (PRIOR ART)

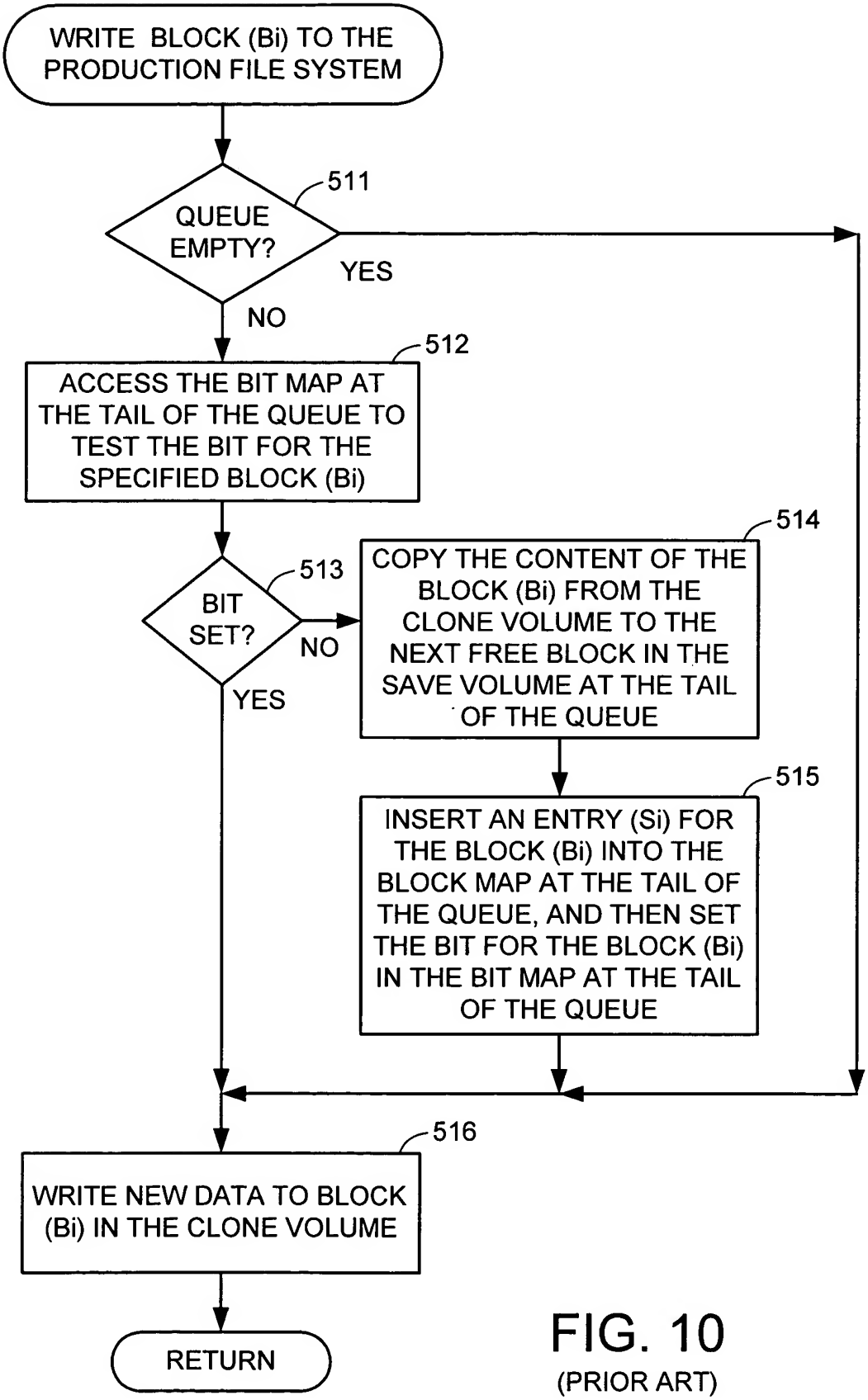

FIG. 10
(PRIOR ART)

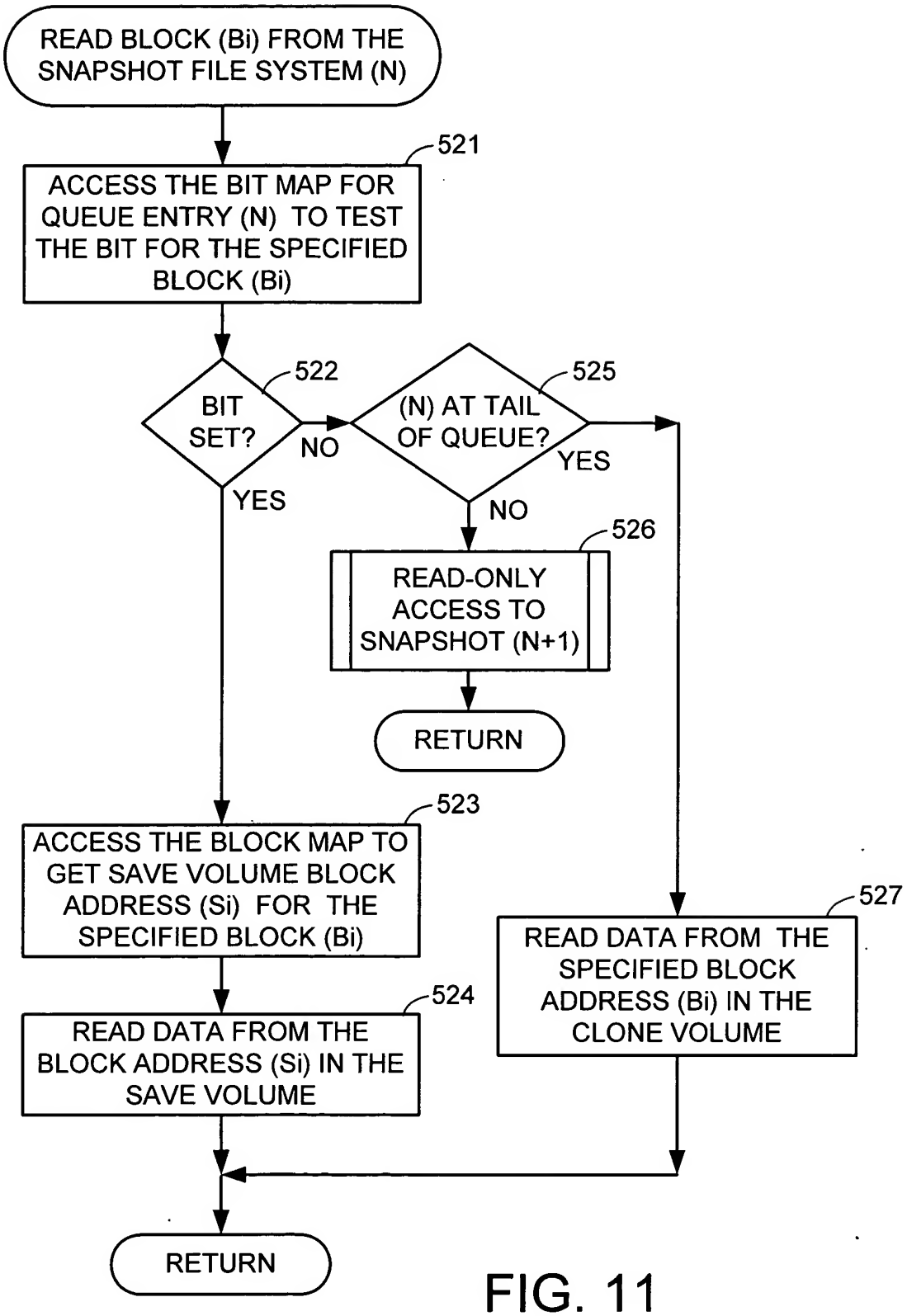

FIG. 11
(PRIOR ART)